# TCD System Configuration

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| Subsystem | Physical Configuration | | | | Software Configuration | | | |
|---|---|---|---|---|---|---|---|---|
| | Slot | VME Address | Group ID | Cable Driver Cards(conn) | Detector ID | Vers # | Intrnl Busy | Acc/Abrt Clear (rhic ticks) |
| | | | | | | | | |
| BBC | 7 | 0x11000000 | N/A | 1(3) | 0xf | 2 | N/A | N/A |
| ETOW | 8 | 0x12000000 | 5 | 1(2) | 0x8 | 6 | | |
| SSD | 9 | 0x13000000 | 0 | 1(2) | 0x5 | 1 | | |
| FPD | 10 | 0x14000000 | 1 | 1(2?) | 0x7 | 5 | | |
| TOF | 11 | 0x15000000 | 2 | 1(4) | 0x4 | 4 | | |
| ESMD | 6 | 0x10000000 | 6 | 1(7) | 0x9 | 5 | | |
| TPC | 13 | 0x1e000000 | 0 | 3(24) | 0x0 | 8 | | |
| SVT | 14 | 0x16000000 | 0 | 3(24) | 0x1 | 6 | | |
| BSMD/PSD | 15 | 0x19000000 | 4 | 2(20) | 0x2 | 7 | 3.2ms | 2 (both) |
| CTB/ZDC | 16 | 0x1a000000 | N/A | 1(3) | 0xe | 2 | N/A | N/A |
| BTOW | 17 | 0x1b000000 | 3 | 1(9) | 0x6 | 4 | 14ms | 2(both) |
| FTPC | 18 | 0x1c000000 | 0 | 1(4) | 0x3 | 7 | | |
| PMD | 19 | 0x1d000000 | 7 | 0(1) | 0xa | 2 | | |
| | 20 | | | | | | | |
| | 21 | | | | | | | |

**Subsystem**

There is one row in this table for every subsystem that uses a TCD module to distribute clocks and triggers.

**Physical Configuration**

TCD-Crate Slot

This column describes which slot in the 9U VME crate currently holds this specific TCD

Base Address

The VME base address of this TCD

Group ID

The jumper setting on the TCD that determines which bit in the trigger detector bitmask this TCD will respond to and which busy bit it will drive. The BBC, CTB and ZDC are fast trigger-only detectors that do not receive triggers and are never busy so they have no jumpers and are not members of any group.

Number of Cable Driver Cards

Each TCD drives one output cable. That cable can multi-drop to one or more Cable Driver Cards housed in a 6U crate underneath the TCD crate. The number of cards varies depending on the number of drops, listed in parenthesis, needed by the subsystem. Each Card can drive up to 8 outputs.

**Software Configuration**

Detector ID

This is the ID number of the customizable code that is loaded into the FPGA on each TCD module.

FPGA Code Version Number

The FPGA programming for some Detector IDs has been through several iterations. This is the version number of the code that is currently loaded in the FPGA.

NOTE: The Detector ID and Version Number can be read from any TCD using a 16-bit read of the register at address offset 0x1e. The Version Number is coded into bits 0:11 and the Detector ID is in bits 12:15